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Claims

[c1] 1.A structure comprising:
a base region having a monocrystalline region located atop a Si substrate and a polycrystalline region located atop trench isolation regions that are present in the substrate;
a raised extrinsic base located atop the of the polycrystalline region and part of the monocrystalline region;
a silicide region located atop the raised extrinsic base; and
an emitter located atop the monocrystalline region which is spaced apart and isolated from the raised extrinsic base and the polycrystalline regions of the base region, wherein the silicide region atop the raised extrinsic base extends to the emitter in a self-aligned manner.

[c2] 2.The structure of Claim 1 wherein said base region comprises Si, SiGe or a combination thereof.

[c3] 3.The structure of Claim 1 wherein said raised extrinsic base comprises a doped semiconductor layer.

[c4] 4.The structure of Claim 3 wherein said doped semiconductor layer comprises polysilicon, Si or SiGe.

[c5] 5.The structure of Claim 1 wherein said silicide region comprises a refractory metal.

[c6] 6.The structure of Claim 5 wherein said refractory metal is Ti, W, Co or Ni.

[c7] 7.The structure of Claim 1 wherein said emitter comprises polysilicon.

[c8] 8.The structure of Claim 1 wherein said emitter is T-shaped.

[c9] 9. The structure of Claim 1 wherein said silicide region is located in an undercut region that is located beneath an upper portion of the emitter.

[c10] 10.A method of forming a high-performance hetero-junction bipolar transistor comprising the steps of:
forming a base region atop a Si substrate having trench isolation regions and a collector located therein, said base region including a monocrystalline region atop the Si substrate and a polycrystalline region atop the trench isolation regions;
forming an oxide layer atop the base region;
forming an emitter pedestal region atop the oxide layer located atop the monocrystalline region;
forming a raised extrinsic base adjacent to said emitter

pedestal region;

forming a silicide layer atop the raised extrinsic base; and

forming an emitter in said emitter pedestal region, said emitter is spaced apart and isolated from the raised extrinsic base and the silicide layer, wherein said silicide layer atop the raised extrinsic base extends to the emitter in a self-aligned manner.

[c11] 11.The method of Claim 10 wherein said step of forming the base layer comprises an epitaxial growth process that is performed at a temperature of from 450°C to 700°C.

[c12] 12.The method of Claim 10 wherein said step of forming said oxide layer comprises an oxidation process or deposition.

[c13] 13.The method of Claim 10 wherein said step of forming said emitter pedestal region comprises the steps of: depositing a polysilicon layer atop said oxide layer, depositing a nitride layer atop the polysilicon layer and patterning the polysilicon and nitride layer to form a material stack atop the oxide layer.

[c14] 14.The method of Claim 13 further comprising forming insulating spacers on exposed sidewalls of said material

stack.

[c15] 15.The method of Claim 10 wherein said step of forming the raised extrinsic base comprises providing a doped semiconductor layer on at least said polycrystalline regions of said base layer.

[c16] 16.The method of Claim 15 wherein said doped semiconductor layer is formed by an in-situ doping deposition process.

[c17] 17.The method of Claim 10 wherein said step of forming the silicide layer comprises the steps of: forming a refractory metal atop the raised extrinsic base and annealing at a temperature to provide the silicide layer.

[c18] 18.The method of Claim 17 wherein said annealing is performed using a single annealing step.

[c19] 19.The method of Claim 10 wherein said step of forming the emitter comprises selectively removing portions of the emitter pedestal region to provide an emitter opening to the monocrystalline region of the base and forming an emitter polysilicon in at least said emitter opening.

[c20] 20.The method of Claim 10 further comprising a polysilicon chemical mechanical polishing step between the

steps of forming the raised extrinsic base and forming the silicide layer.

[c21] 21.The method of Claim 10 further comprising an oxide chemical mechanical polishing step between the steps of forming the silicide layer and forming the emitter.

[c22] 22.A method of forming a high-performance hetero-junction bipolar transistor comprising the steps of:
providing a structure comprising at least a raised extrinsic base region and an emitter pedestal region, said emitter pedestal region located on a portion of a base region that is monocrystalline;
forming a stack comprising a sacrificial oxide layer and a top nitride layer on said raised extrinsic base region;
removing layers of at least the emitter pedestal region to provide an opening that exposes the monocrystalline base region;
forming an emitter in said opening;
forming an isolation nitride spacer on sidewalls of at least said emitter;
forming an undercut in an area beneath the emitter;
depositing a conformal refractory metal; and
annealing said conformal refractory metal whereby said annealing causes reaction between the conformal refractory metal and underlying Si so as to form a metal silicide region atop the raised extrinsic base that extends to

said emitter in a self-aligned manner.

[c23] 23.The method of Claim 22 wherein said base region is formed by an epitaxial growth process.

[c24] 24.The method of Claim 22 wherein said removing the layers of at least the emitter pedestal comprises opening the nitride layer by chemical polishing or etching to un-exposed said sacrificial oxide layer; and removing the sacrificial oxide layer by etching thereby exposing the monocrystalline portion of the base region.

[c25] 25.The method of Claim 22 wherein said forming said emitter comprises depositing an emitter polysilicon and a nitride cap; and patterning said emitter polysilicon and nitride cap by lithography and etching.

[c26] 26.The method of Claim 25 wherein said raised extrinsic base is patterned with said emitter polysilicon and said nitride cap.

[c27] 27.The method of Claim 22 wherein said forming said undercut comprises a chemical oxide removal process or an equivalent wet etch process.

[c28] 28.The method of Claim 22 wherein said emitter is T-shaped and said undercut is formed beneath upper portions of the T-shaped emitter.

[c29] 29.The method of Claim 22 wherein following said annealing unreacted conformal refractory metal is removed.

[c30] 30.The method of Claim 22 wherein said metal silicide region has an inner edge that located beneath an upper T-shaped portion of said emitter.